REMARKS

The final Office Action of **February 26, 2003**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the final Office Action.

Claims 1-38 were pending in the present application prior to the above amendment, with claims 10-27 being withdrawn from consideration. By the above amendment, claim 1 has been amended and claim 32 has been canceled. Applicant submits that no issue of new matter is set forth by the aforementioned amendment since the amended subject matter added to claim 1 finds support at least at page 6, line 25, to page 7, line 13, as well as page 21, line 25, to page 22, line 5, of the specification. Accordingly, claims 1-31 and 33-38 are presently pending, of which claims 1-9, 28-31 and 33-38 are allowable over the prior art.

Claims 1, 3, 28, 32, 33 and 34 are rejected, under 35 U.S.C. §103(a), as unpatentable over U.S. Patent No. 6,093,951 to Burr ('951); while 2 and 29 are rejected, under 35 U.S.C. §103(a), as unpatentable over Burr in view of in view of the U.S. Patent No. 5,177,569 to Koyama et al ('569), claims 4-9, 30, 31 and 35-38 are rejected, under 35 U.S.C. §103(a), as unpatentable over the alleged Admitted Prior Art (APA) in view of Burr ('951) and Koyama et al ('569) and claim 6 is rejected, under 35 U.S.C. §103(a), as unpatentable over U.S. Patent No. 4,476,622 to Cogan ('622) in view of the U.S. Patent No. 5,869,359 to Prabhakar ('359). The Applicant respectfully contends that the presently claimed subject matter clearly defines over the cited references for at least the following reasons.

Amended claim 1 is directed generally to a semiconductor device comprising an epitaxial semiconductor substrate having an epitaxial region of silicon formed by epitaxial growing silicon on a silicon substrate included in at least an upper portion thereof; and a diffusion layer formed in said epitaxial region by using a dopant ion having a relatively large mass number, wherein said diffusion layer is formed shallower than said epitaxial region.

Accordingly, the crystal quality of the epitaxial region grown on the silicon substrate is superior. Hence, as compared to a semiconductor obtained by the general rotational pulling (Cz) method, EOR (end-of-range) dislocation loop defects are reduced, and heavy ions are minimally segregated in a region below an amorphous-crystal interface. As a result, the semiconductor device can be refined with a leakage current derived from the segregated suppressed as discussed at page 6, line 25, to page 7, line 11, of the present specification.

In contrast to claim 1, Burr teaches (column 12, line 60 to column 15, line 40; Fig. 5G), forming a retrograde pocket region 347 in a substrate 332 by ion implantation. Burr further teaches (column 14, line 36), that indium can be used as an dopant of the region 347.

Burr also teaches that in Process I, the substrate 332 is a monocrystalline silicon or a suitable semiconductor material (column 13, lines 8-9), but fails to disclose that the substrate 332 is a laminated structured epitaxial semiconductor substrate having an epitaxial region formed by epitaxial growing silicon on a silicon substrate.

Further, in Process II (column 15, line 47 to column 16, line 19), Burr discloses:

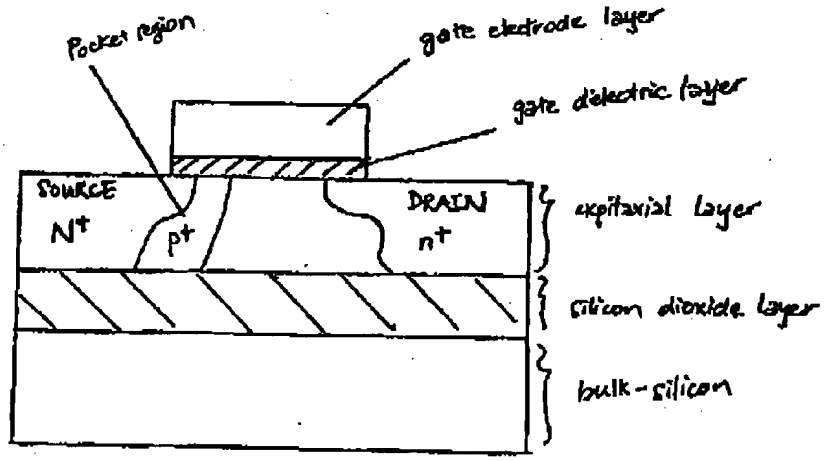
a) a step of forming a pocket region by ion implanting boron,

b) a step of forming an epitaxial silicon layer having a thickness of 50-200 angstroms (5-20nm), after the step a), and

c) a step of forming a gate insulating film and a gate electrode on the epitaxial silicon layer, after forming the pocket region and the epitaxial layer.

Since the epitaxial layer is formed on the substrate 332 after the formation of the pocket region, the pocket region is formed under the epitaxial layer. Hence, according to the process II of Burr, it is technically impossible to form the pocket region shallower than the epitaxial layer.

Finally, Burr (column 16, lines 20-41) further discloses forming, on a silicon dioxide layer, a device element in a SOI structure composed of an epitaxial layer having a thickness of 70-2000 angstroms (7-200nm). However, this is different from the amended claim 1 of the present invention for the following reasons. Initially, it is noted that Burr completely fails to disclose forming a pocket region which is shallower than the epitaxial layer in the epitaxial layer. Moreover, since the thickness of the epitaxial layer is 7-200 nm, it is technically very difficult to form the pocket region shallower than the epitaxial layer of 7-200 nm. In addition, in a SOI structure, since the silicon dioxide layer is provided under the epitaxial layer, as shown in the Reference Figure below (which recreates the SOI structure of Burr), each bottom portion of the source, drain and pocket region should be connected to the silicon dioxide layer. This is because, if the source, drain and pocket region are formed shallower than the epitaxial layer, the pn-junction capacitance increases and the usefulness of the SOI structure decreases. Hence, if the source and pocket region in the SOI structure is formed as shown in the Reference Figure, the pocket region has a same depth as the epitaxial layer and is not shallower than the epitaxial layer.



REFERENCE FIG.

Additionally, the epitaxial semiconductor substrate in the amended claim 1 has an epitaxial region formed by the epitaxial growth of silicon on a silicon substrate. In

this case, since the epitaxial layer is formed directly on the silicon substrate, as described above, the crystal quality of the epitaxial region will be superior, and EOR dislocation loop defects are reduced during the forming of the diffusion layer by heavy ions implantation. On the other hand, since the silicon dioxide layer is provided under the epitaxial layer in the SOI structure of Burr, it is generally known that the crystal quality is inferior to even that of the general silicon substrate. Hence, the epitaxial layer of the SOI structure is inferior to that of the epitaxial region formed on the silicon substrate in the amended claim 1, and cannot achieve the effect of the present invention.

As described above, since Burr fails to teach or suggest forming a diffusion layer shallower than the epitaxial layer, on the epitaxial region formed by epitaxial growing silicon on a silicon substrate, employing dopant ions having relatively larger mass number, the amended claim 1 is patentable over Burr alone. Consequently, the rejection of claims 1, 3, 28, 32, 33 and 34, under §103(a), is improper and must now be withdrawn.

With regard to the claim 6, the claim recites a heavily-doped diffusion layer formed, by using a dopant ion having a relatively large mass number, in a semiconductor substrate having a <110>- oriented zone axis.

Since the device uses the semiconductor substrate having a plane orientation of (110), thus the <110>-oriented axis, the implanted heavy ion is channeled and collides less with a silicon atom, resulting in reducing implantation damage of the semiconductor substrate. As discussed in the specification at page 15, lines 15-23, and Embodiment 4, formation of lattice interstitial silicon is suppressed and EOR dislocation loop defects are reduced, so that heavy ions can be minimally segregated in the region below the original amorphous-crystal interface, and leakage current derived from the segregation can be suppressed. Also, even when the heavy ion is channeled, the implantation range is less largely increased owing to the mass effect of the heavy ion versus that of a light ion, and hence, shallow junction can be realized.

In contrast to claim 6, the Applicant's Admitted Prior Art (APA) teaches forming a diffusion layer by implanting indium into a semiconductor substrate having a <100>- oriented zone axis. However, the APA fails to disclose forming a diffusion layer by implanting heavy ion into a semiconductor substrate having a <110>-oriented zone axis. To remedy this deficiency, the Examiner relies upon the teachings of Burr and Koyama et al. In that regard, Burr teaches forming a pocket diffusion layer by implanting indium into a semiconductor substrate, but fails to teach or suggest about the zone axis (plane orientation) of the semiconductor substrate. The Koyama et al reference (Figure 7, element 14) teaches that a gate electrode can comprise a polycrystalline silicon layer 14 composed of crystal grains having different plane orientations of (111) and (110). During ion implantation of a dopant using the gate electrode as a mask, if boron ions are implanted into the polycrystalline silicon layer 14, the implanted boron ions reach the semiconductor substrate by penetrating the polycrystalline silicon layer 14, thus causing the channeling effect.

According to Koyama et al, in order to solve the problem, a gate electrode (Figure 2, 3D, elements 4, 5) is composed of a polycrystalline silicon layer 4 having a plane orientation of (110) and a monocrystalline silicon layer 5 having a plane orientation of (110). However, Koyama et al (column 6, lines 45-46) disclose a silicon substrate 1 having a plane orientation of (100). Therefore, other than teaching one of skill in the prior art to employ a gate electrode composed of a polycrystalline silicon layer and a monocrystalline silicon layer each having a plane orientation of (110) and a substrate of a (100) orientation, Koyama et al provides no guidance to one of ordinary skill in the prior art to structure the substrate to have a <110> orientation as claimed.

This same analysis applies to the combination of teachings of Burr with Koyama et al. That is, according to Koyama et al, the (110) plane orientation of the monocrystalline silicon layer 5 is only a part of the gate electrode 10, and is not a plane orientation of the silicon substrate 1. Moreover, as discussed above, Koyama et al disclose that the plane orientation of the silicon substrate is (100). Consequently,

the combination of teachings of Koyama et al with either the APA or Burr does not teach or suggest each of the features claimed.

Finally, Koyama et al merely disclose the monocrystalline silicon gate electrode layer 5 having the (110) plane orientation to prevent boron ions, which have a relatively small mass number, from penetrating the gate electrode and reaching the silicon substrate, but fails to teach or suggest about the case when heavy ions are used. In addition, the problem of the penetration of boron ions exists only in the gate electrode and not in a pocket diffusion layer formed on the silicon substrate. Therefore, there is no suggestion/motivation in Koyama et al for combining the zone axis of the substrates in APA and Burr with the (110) plane orientation of the gate electrode in Koyama.

Consequently, the rejections of claims while 2 and 29, under §103(a), as unpatentable over Burr in view of Koyama et al, and claims 4-9, 30, 31 and 35-38, under §103(a), as unpatentable over the alleged Admitted Prior Art in view of Burr and Koyama et al, have been set forth in error and must now be withdrawn.

With regard to the rejection of claim 6, under §103(a), over Cogan in view of Prabhakar, Cogan teaches a method for forming a diffusion layer 44 by implanting arsenic into an epitaxial layer 40 having a plane orientation of (110). However, Cogan fails to teach or suggest about implanting heavy ions, such as In or Sb. The Prabhaker reference teaches (Figure 4), a method for forming an etch stopper layer 30 by ions implanting antimony into a SOI layer 16. However, in the step following ion implantation of the etch stopper layer (see Figure 5), the etch stopper layer 30 is removed during the forming of a trench 28. In other words, the etch stopper later 30 is transitory in nature and is only provided for the purpose of forming the trench 28, and is not formed as a device diffusion layer. Accordingly, the etch stopper layer 30 formed by implanting heavy ion and removed thereafter, as disclosed in Prabhaker, has a different purpose from the device diffusion layer 44 disclosed in Cogan. Therefore, there is no suggestion or motivation provided by Prabhakar to form a

diffusion layer by implanting heavy ions, such as In or Sb, in the diffusion process of Cogan. Consequently, the rejection of claim 6, under §103(a), is also improper and must be withdrawn.

CONCLUSION

Having responded to all rejections set forth in the outstanding non-Final Office Action, it is submitted that claims 1-9, 28-31 and 33-38 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Lastly, it is noted that a separate Extension of Time Petition (two months) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740819-560).

Respectfully submitted,

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